A Single-Chip Digital Phase Meter For Vibration Analysis Of Rotating Machinery

Michael Lindig Bös
Director del CIDETEC - IPN
e-mail: mlindig@vmredipn.ipn.mx

The design of a digital phase meter, intended for vibration monitoring and analysis of electric power generators, is discussed. The design may be implemented in a single, field-programmable gate array, operating at 32 MHz. Inputs to the device are a trigger pulse and a sampled, bandlimited vibration signal. The device measures the phase angle of the signal at 1/2, 1 or 2 times the rotation frequency with a resolution of 1 degree, referred to the trigger signal. A novel frequency multiplier, as well as a tracking filter and zero-crossing detector are incorporated into the device. The trigger frequency range is 1 to 1000 Hz. A detailed error analysis, as well as experimental results, are presented.

I. Introduction

The monitoring and performance analysis of electric power generators is of great practical interest. The process involves the real-time processing of vibration signals and the measurement of several parameters, such as peak-to-peak amplitude and phase angle of the different harmonic components of the vibration signal as referred to a trigger signal obtained from the same machine.

In this work, the design of a digital phase meter is presented. The target specifications of the design are as follows:

Rotating speed:	60 to 60,000 rev/min.
Resolution:	1 degree
Precision:	± 1 degree at 0.5 and 1 times the frequency of rotation, ± 2 degree at 2 times the frequency of rotation.

The input signal to the device is a vibration signal, sampled at 102.4, 51.2, 25.6 or 10.24 KHz and bandlimited at 1/2.56 the sampling frequency. The target specifications apply to a signal amplitude range of 10 to 1.

A key component for the monitoring process is the tracking filter. The vibration signal is sampled at N times the frequency of rotation, where N is the desired angular resolution. The sampling frequency is obtained by a digital frequency multiplier that measures the time interval between successive trigger pulses, and the sampled signal is then filtered by a phase-compensated bandpass filter whose bandpass region is centered at $2\pi k/N$, where k is the desired harmonic component. Peak-to-peak amplitude and phase measurements may be obtained from the filtered signal, the latter by means of a zero-crossing detector.

Since the lowest practical bandpass centre frequency obtainable by a digital filter is limited both by the filter order and, for fixed-precision calculations, by the word size of the processor, higher resolution phase measurements are usually obtained by means of an interpolation process.

In what follows, a block diagram of the design and specifications of each functional unit are given. A performance analysis is presented, concentrating on the following aspects:

1.- The error generated by sampling two times the same signal at different sampling frequencies.
2.- The violation of the sampling theorem at low frequencies of rotation.
3.- The oversampling incurred in at high speeds of rotation.

Results of computer simulations for several signal qualities of the vibration signal are shown. Actual measurements validate, within the resolution of the available equipment, these simulations.

II. Circuit Description

A block diagram of the relevant processing elements is shown in **figure 1.** The input signal, f(t), is amplified and bandlimited. The output of the lowpass filter feeds a 12-bit analog to digital converter. The resulting sampled signal, f(n), is one of two inputs to the phase meter. The other is a synchronization pulse (SYNC), occurring once for each rotation of the machine under study. The phase meter operates at a frequency given by a master clock (CLK), here, a 32 MHz oscillator. The main functional elements of the phase meter (enclosed by a dashed line) are a frequency multiplier, an 8th. order IIR filter, a zero-crossing detector and a counter. A peak-to-peak detector is included in the design, as well as a system bus interface. The filter coefficients and partial processing results are stored in a static RAM, which in the prototype is an external device. The filter coefficients are completely programmable by means of the system bus. In what follows, the main functional elements will be described in more detail.

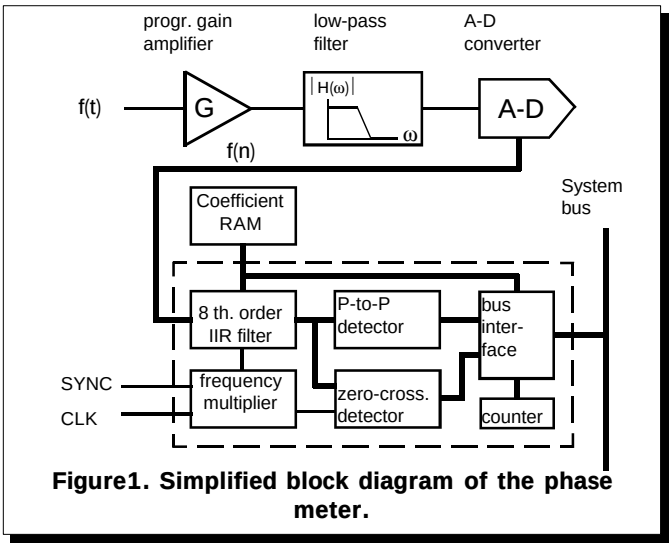

Figure1. Simplified block diagram of the phase meter.

II.1 The frequency multiplier.

Ideally, this functional element generates an output pulse train whose frequency is given by $f_{OUT} = Nf_{IN}$, where f_{IN} is the input signal frequency and N a positive integer [1], [2]. Let τ_{OUT} be the period of the output signal. Since τ_{OUT} is derived from the system clock and constraint to be an integer number of system clock periods, the multiplication can, in general, not be realized exactly. A detailed description of the design solution used can be found in [3]. For applications where the output signal is used to sample a periodic signal harmonically related to the input signal of the frequency multiplier, it has been shown that the maximum amplitude error is given by $\varepsilon(n)_{max} < 2\sin(\pi/K)$, where $K = f_{CLK}/f_{IN}$. Also, the frequency multiplier introduces a delay of, at most, 1 sample interval.

In the present application, the frequency multiplier operates at 1/2 the system clock frequency (16 MHz), and the maximum input frequency is 2KHz. For these values, the maximum amplitude error is 0.0393%, and the phase error introduced is at most 0.045 degrees. These errors are more than one order of magnitude smaller than the target specifications, and, in what follows, will be neglected.

II.2 The IIR filter.

The device implements 4 cascaded second-order sections, as shown in **figure 2**. The index j designates the section number, a_{jk} and b_{jk} are filter coefficients and $w_{jk}(n)$ represent intermediate sequences. The structure is known as the transposed direct form II [4] and has the property of minimizing the storage requirements for a given filter order. The section is general, in the sense that lowpass, bandpass, highpass and allpass transfer functions can be realized. The design is based on fixed 16-bit precision, two's complement arithmetic. Values in the range $-2 \le x \le 2 - 2^{-14}$ may be represented.

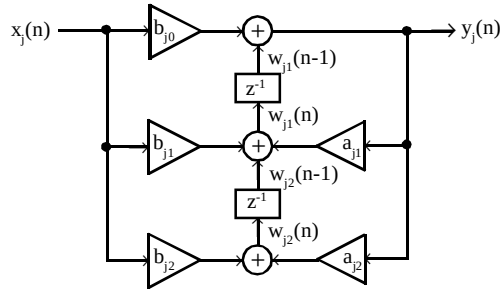

Figure2. A second-order filter section.

In the present application, it is assumed that a fourth order bandpass Butterworth filter, followed by an allpass filter of the same order, is implemented. For the fundamental frequency component of the input signal, the filter was designed with a passband of $1.9\pi/45 \le \omega \le 2.1\pi/45$, using a commercial software package [5]. The allpass network was designed for a constant overall delay of 45 samples. **Figure 3** shows the frequency response of the filter. The maximum amplitude error in the passband region is 0.77%. No measurable phase error in the passband was observed.

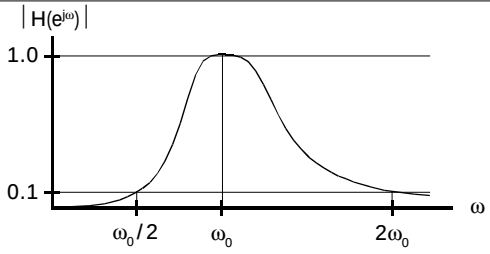

Figure3. Frequency response for $w_0 = 2p/45$

II.3 Peak-to-peak and zero crossing detectors.

The peak-to-peak amplitude and phase measurements are derived from the output samples of the filter, y(n). For a given input period, and for each sample interval, the value p(n) = y(n) - y(n-1) is calculated. If p(n), y(n) and y(n-1) are all positive and p(n+1) is negative, y(n) is stored as the positive peak value. Similarly, if p(n), y(n) and y(n-1) are all negative and p(n+1) is positive, y(n) is stored as the negative peak value. The sum of the magnitudes of both peak values is reported at the occurrence of the next SYNC pulse.

The event of zero crossing is defined to occur during the sample period between samples y(n) and y(n-1), such that $y(n) \geq 0$ and $y(n-1) < 0$. Note that the sampling intervals are synchronized to the SYNC pulse. Since the sampling period equals 8 degrees, linear interpolation is used to achieve the desired 1-degree resolution. Specifically, the device implements the recursion:

$\delta(k+1) = \delta(k) - [y(n) + |y(n-1)|]$, with
$\delta(0) = 8\,|y(n-1)|$

for all values of k such that $\delta(k) > 0$.

That is, the expression $[8\,|y(n-1)|]/[y(n)+|y(n-1)|]$ is evaluated by successive substractions. Clearly, the final value of k equals the integer part of the expression given above. This value is added to 8 times the count of sampling intervals between the occurrence of a SYNC pulse and the sample y(n-1), thus yielding the phase angle in degrees.

III. Error Analysis

Let f_R be the frequency of rotation of the machine. Then, $Nf_R = f_M$ is the output frequency of the frequency multiplier. Denote by f_m the sampling frequency. Two situations may be distinguished, namely either $f_M \leq f_m$, or $f_m < f_M$. If $f_M \leq f_m$, the vibrations signal is, in general, not bandlimited in terms of f_M. Also, since both sampling frequencies are uncorrelated, there will be an error due to the uncertainty of the precise sampling instant. On the other hand, if $f_m < f_M$, the (sampled) vibration signal is oversampled. In what follows, bounds on these sources of error will be established. Because of space limitations, only the fundamental frequency component of the vibration signal will be considered, that is, $f(t) = \sin(2\pi f_R t)$.

III.1 Error due to uncertainty in the sampling instants

If f(t) where sampled by the output of the frequency multiplier, the sampling interval would be $(f_m/f_M)\tau_m$, where $\tau_m = 1/f_m$. Since f(t) is already sampled at τ_m intervals, the signal can be observed only at integer multiples of (f_m/f_M). Denote by $\lfloor x \rfloor$ the greatest integer less or equal to x. Define an error signal, $\varepsilon(n)$:

$$\varepsilon(n) = \sin 2\pi(nf_m/f_M)\tau_m - \sin 2\pi\lfloor nf_m/f_M \rfloor \tau_m \quad \ldots\ldots 1$$

for n a positive integer.

Since $(nf_m/f_M) < \lfloor nf_m/f_M \rfloor + 1$ for all n, and using a trigonometric identity, from (1) results:

$$\varepsilon(n) < 2\sin(\pi\tau_m)\{\cos\pi\tau_m[(2nf_m/f_M) - 1]\} \quad 2$$

and it follows that:

$$\varepsilon(n)_{max} < 2\sin\pi\tau_m \quad \ldots\ldots 3$$

At the lowest sampling frequency (10.24 KHz), the amplitude error given by (3) is 0.0614%. The delay introduced by the double sampling process is clearly less than τ_m. Since the sampled signal is further processed by a bandpass filter, it is reasonable to assume that at its output the delay tends toward a mean value. This has been confirmed by experiment. The mean delay is, of course:

$$\delta(n)_{AV} = (\tau_m/N) \quad [(nf_m/f_M) - \lfloor nf_m/f_M \rfloor] \quad \ldots\ldots 4$$

It can be shown that, for f_m/f_M not an integer,

$$0.25\tau_m \leq \delta(n)_{AV} < 0.5\tau_m$$

Taking the lower bound as a systematic error, it follows that for phase errors of less than 1 degree, $f_R < 360/4f_m$. For the sampling frequencies specified, the upper limit on the rotating speed is, respectively, 1138, 569, 284 and 114 rev/sec.

III.2 Error due to aliasing

Assume the input to a bandpass filter with center frequency $2\pi/N$ is a periodic, non-bandlimited signal, with frequency components located at $2\pi n/N$, $n = 0,1,....$ Then, the output of the filter contains frequency components located at $2\pi/N$, $2k\pi(N-1)/N$ and $2k\pi(N+1)/N$, where $k = 1, 2,....$

The amplitude spectrum of physical signals decreases at increasing signal frequencies, according to a rate of the form $1/\omega^{\alpha}$. That is, the normalized amplitude of the aliased frequency components is $1/(kN-1)^{\alpha}$ and $1/(kN+1)^{\alpha}$, respectively. The sum of these amplitudes is, then:

$$\sum_{k=1}^{\infty}\left[\frac{1}{(kN-1)^{\alpha}}+\frac{1}{(kN+1)^{\alpha}}\right] \approx \frac{2}{N^{\alpha}}\sum_{k=1}^{\infty}\frac{1}{(k)^{\alpha}} \qquad .....5$$

Now, the sum in (5) converges for $\alpha > 1$. For vibration signals, α can be taken to be ≥ 2. In particular, for $\alpha = 2$, the sum converges to $\pi^2/6 \approx 1.645$ [6]. For $N = 45$, the sum of the amplitudes of the aliased frequency components is then 0.00162, and the worst-case phase error is 0.093 degrees.

III.3 Error due to oversampling the sampled signal

If $f_m < f_M$, during a sample period $1/f_m$ a certain number of consecutive samples taken at $1/f_M$ intervals will have equal values. Assume $f_M/f_m = R$ to be an integer. Then, the oversampling process may be modelled as a simple FIR filter of order R-1, shown in **figure 4**.

The Z-transform of the transfer function is given by:

$$H(z) = \sum_{r=0}^{R-1} z^{-r} = \frac{1-z^{-R}}{1-z^{-1}} \qquad .....6$$

And the frequency response is easily obtained as:

$$H(e^{j\omega}) = e^{-j\omega(R-1)/2}\,\frac{\text{sen}\,\omega R/2}{\text{sen}\,\omega/2} \qquad .....7$$

That is, oversampling has a lowpass filter effect and introduces a delay of (R-1)/2 samples. Ec. (7) gives average values if R is not an integer, because for any given input sample period $1/f_m$, the number of equal samples obtained at the rate $1/f_M$ is an integer (either $\lfloor R \rfloor$, or $\lfloor R \rfloor + 1$).

In the present application, the maximum oversampling rate is $N(f_R)_{max}/(f_m)_{min}$, that is, 4.395. From (7), and for $\omega = 2\pi/45$, the attenuation is $|H(e^{j\omega})|/4.395 = 0.985$, and the delay 1.697 samples, or 13.578 degrees. This delay can be corrected, since the sampling frequency is known, and the rotation frequency is measured by the frequency multiplier.

III.4 Error due to noise

The phase angle measurement error due to this source depends on the type and specifications of the bandpass filter. Clearly, in order to reduce this error, a narrow bandpass region is desirable. On the other hand, the filter parameters are influenced by the maximum expected acceleration of the rotation frequency. Let $\tau_{IN}(n)$ be the period of rotation. The output of the frequency multiplier is, then, $\tau_{IN}(n-1)/N$, that is, the output frequency is defined by the previous input period. Hence, if the machine accelerates, the centre frequency of the passband filter is no longer coincident with the frequency of rotation and the filter cannot be to narrow in the passband.

Computer simulations have been performed for various synthetic signals, and for the filter specified in II.2. Specifically, the phase error due to added noise signals of uniform distribution and zero mean was measured (**figure 5**). The observed variance of the phase error increases linearly with the variance of the noise signal, reaching 1 degree for a noise with a standard deviation of 0.212.

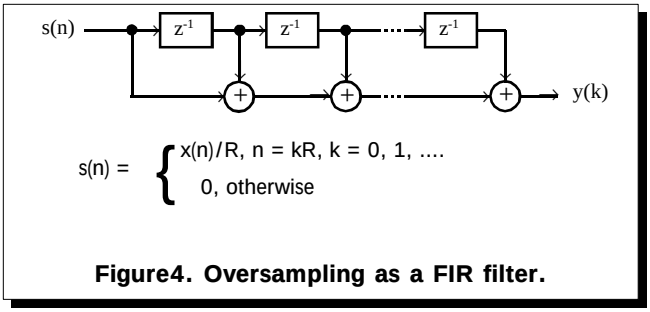

Figure4. Oversampling as a FIR filter.

IV. Physical Implementation

A 4-channel prototype was built, based on 2 field-programmable gate arrays type A1280XL from ACTEL [7], providing each the equivalent of 20,000 gates. The functional unit requiring most resources is, of course, the multiplier used in the implementation of the digital filter. In order to minimize these resources, a simple shift-add

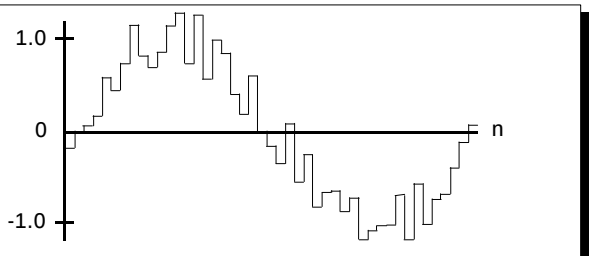

Figure5. Vibration signal with additive noise, s=0.2

algorithm was used. Each multiplication is executed in 16 clock cycles, that is, the second-order section shown in fig. 2 executes in 80 clock cycles. It is estimated that a single-channel design, operating at 32 MHz, could be implemented in a single FPGA and one external static RAM. The storage requirements depend on the filter order. For each second-order section, 7 16-bit words, or 14 bytes, are required. The prototype implements an 8-bit memory interface, and, for ease of design, uses 16 bytes for each second-order section.

V. Conclusions

The design of a digital phase meter has been presented, that lends itself well to single-chip implementations. The design objectives have, in general, been satisfied. The interpolation algorithm of the phase measurement has yet to be refined by increasing its resolution, and providing rounding instead of simple truncation. The most important source of error is the delay introduced by the double sampling process. This delay can, however, be calculated, since both the sampling frequency and the output frequency of the frequency multiplier are known for each input signal period.

Another important error is the aliasing error, especially at low input frequencies. This suggests the use of higher values of the multiplication factor N (see ec. 5), and, hence, higher-order passband filters. If a 5th-order filter operating at a bandpass centre frequency of $2\pi/90$ where implemented, the design objectives would be exceeded. For the design solution discussed, this means an increase of the operating frequency from 32, to 40 MHz.

References

[1] H.Y. Lo, J.H. Lu. "A simple design for a digital programmable frequency multiplier". *Int. J. Electron.*, vol 46 no. 5, pp.535-5542, Dec. 1979.

[2] N. Boutin, A. Boucher. "A novel digital frequency multiplier". *IEEE Trans. Instrum. Means.*, vol 35 no. 4, pp.556-570, Dec. 1986.

[3] M. Lindig Bös. "A simple, high-precision, high-speed digital frequency multiplier". *Proceedings of the 40th Midwest Symposium on Circuits and Systems*, Sacramento, Cal., Aug.3-6, 1997.

[4] Oppenheim, A.V., Schafer, R.W. "Digital Signal Processing". *Prentice-Hall,* 1975.

[5] DFDP3/plus Instruction Manual. Atlanta Signal Processors, Inc., 1992.

[6] Knopp, K. "Infinite Sequences and Series". *Dover*, 1956.

[7] FPGA Data Book and Design Guide. ACTEL Corp., 1995.